

Claims

[c1] What is claimed is:

1. An apparatus for parallel calculation of prediction bits for a spatially predicted coded block pattern having an A0 bit, an A1 bit, an A2 bit, and an A3 bit, the apparatus comprising:

a storage device storing rows of bits including the spatially predicted coded block pattern, a D0 bit, an X0 bit, an X1 bit, a Y0 bit, and a Y1 bit;

a first circuit connected to the storage device for setting the A0 bit;

a second circuit connected to the storage device for setting the A2 bit;

wherein the first circuit and the second circuit operate in parallel.

[c2] 2. The apparatus of claim 1 wherein the storage device comprises a shift register and after a first clock cycle, the shift register is shifted and the first circuit and the second circuit are used for setting the A1 bit and the A3 bit respectively in a second clock cycle.

[c3] 3. The apparatus of claim 1 wherein the first circuit comprises:

a first comparator connected to the storage device for indicating when the D0 bit and the X0 bit are equivalent; and
a first multiplexer connected to the storage device for selectively setting the A0 bit equal to the X0 bit or the Y0 bit depending on the output of the first comparator.

[c4] 4.The apparatus of claim 3 wherein the second circuit comprises:
a second comparator connected to the storage device for indicating when the X0 bit and the Y0 bit are equivalent;
a first NOR-gate having inputs connected to the output of the first comparator and the output of the second comparator; and
a second multiplexer connected to the storage device for selectively setting the A2 bit equal to the Y1 bit or the X0 bit depending on the output of the first NOR-gate.

[c5] 5.The apparatus of claim 1 wherein the second circuit comprises:
a second comparator connected to the storage device for indicating when the A0 bit and the Y0 bit are equivalent; and
a second multiplexer connected to the storage device for selectively setting the A2 bit equal to the Y1 bit or the A0 bit depending on the output of the second comparator.

- [c6] 6.The apparatus of claim 1 further comprising:
a third circuit connected to the storage device for setting the A1 bit;
a fourth circuit connected to the storage device for setting the A3 bit;
wherein the first circuit, the second circuit, the third circuit, and the fourth circuit operate in parallel.
- [c7] 7.The apparatus of claim 6 wherein the third circuit comprises:
a third comparator connected to the storage device for indicating when the X0 bit and the X1 bit are equivalent;
and
a third multiplexer connected to the storage device for selectively setting the A1 bit equal to the X1 bit or the A0 bit depending on the output of the third comparator.
- [c8] 8.The apparatus of claim 7 wherein the fourth circuit comprises:
a fourth comparator connected to the storage device for indicating when the X1 bit and the A0 bit are equivalent;
a second NOR-gate having inputs connected to the output of the third comparator and the output of the fourth comparator; and
a fourth multiplexer connected to the storage device for selectively outputting the A2 bit or the X1 bit as the A3

bit depending on the output of the second NOR-gate.

[c9] 9.The apparatus of claim 6 wherein the fourth circuit comprises:
a fourth comparator connected to the storage device for indicating when the A1 bit and the A0 bit are equivalent;
and
a fourth multiplexer connected to the storage device for selectively setting the A3 bit equal to the A2 bit or the A0 bit depending on the output of the fourth comparator.

[c10] 10.A method for parallel calculation of prediction bits in a spatially predicted coded bit pattern having an A0 bit, an A1 bit, an A2 bit, and an A3 bit, the method comprising the following step:
(a) if an X0 bit is equivalent to a D0 bit, setting the A0 bit equal to a Y0 bit and setting the A2 bit equal to a Y1 bit, otherwise setting the A0 bit equal to the X0 bit.

[c11] 11.The method of claim 10 wherein step (a) further comprises if the A0 bit is not equivalent to the Y0 bit, setting the A2 bit equal to the A0 bit.

[c12] 12.The method of claim 10 wherein step (a) further comprises if the X0 bit is not equivalent to the D0 bit and the Y0 bit is not equivalent to the X0 bit, setting the A2 bit

equal to the X0 bit, otherwise setting the A2 bit equal to the Y1 bit.

- [c13] 13.The method of claim 10 further comprising the following step:
 - (b) if an X1 bit is equivalent to the X0 bit, setting the A1 bit equal to the A0 bit and setting the A3 bit equal to the A2 bit, otherwise setting the A1 bit equal to the X1 bit.
- [c14] 14.The method of claim 13 wherein step (b) further comprises if the A1 bit is not equivalent to the A0 bit, setting the A3 bit equal to the A1 bit.
- [c15] 15.The method of claim 13 wherein step (b) further comprises if the X1 bit is not equivalent to the X0 bit and the X1 bit is not equivalent to the A0 bit, setting the A3 bit equal to the X1 bit, otherwise setting the A3 bit equal to the A2 bit.
- [c16] 16.The method of claim 13 wherein step (a) is executed in a first clock cycle and step (b) is executed in a second clock cycle.
- [c17] 17.The method of claim 13 wherein step (a) and step (b) are executed in parallel in the same clock cycle.